AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application. As compared to the prior versions and listings of the claims, Claims 1 and 7 have been amended.

Listing of Claims:

1. (Currently Amended) A semiconductor structure comprising:

a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{\cancel{19}18}/cm^3$ and a thickness t1; and

a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein $t1 > 1.2t2$;

t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region;

t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

2. (Previously Presented) The semiconductor structure of Claim 1 wherein $t1 \geq 2.2t2$.

3. (Previously Presented) The semiconductor structure of Claim 1 wherein t1 = 2.3t2, ± 0.1t2.

4. (Previously Presented) The semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. (Previously Presented) The semiconductor structure of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. (Previously Presented) The semiconductor structure of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

7. (Currently Amended) A semiconductor structure comprising:

a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$; and

a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than 0.3μm, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square;

wherein the set of titanium silicide conductors is formed, in part, by a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{18}/cm^3$.

8. (Previously Presented) The semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array, wherein the 3-D memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip.